Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 1-4, 6-11, 13-17, 19-23, 25-34, 37, 40, 45, and 49. Please amend claims 5, 12, 18, 24, 35, 38, 41, 43, 44, 47, 51, and 57, as follows:

Listing of Claims:

1-4. (Cancelled)

5. (Currently amended) The memory hub of claim 35 [[1]] wherein the non-volatile memory is further coupled to the link ~~high-speed~~ interface.

6-11. (Cancelled)

12. (Currently amended) The memory sub-system of claim 38 [[6]] wherein the plurality of memory devices of the memory module comprises synchronous dynamic random access memory devices.

13-17. (Cancelled)

18. (Currently amended) The memory module of claim 43 [[13]] wherein the plurality of memory devices comprises synchronous dynamic random access memory devices.

19-23. (Cancelled)

24. (Currently amended) The processor-based system of claim 47 [[19]] wherein the plurality of memory devices comprises synchronous dynamic random access memory devices.

25-34. (Cancelled)

35. (Currently amended) A memory hub for a hub-based memory sub-system, comprising:

a link ~~high-speed~~ interface for receiving memory access requests;

an electrically programmable non-volatile memory having memory module configuration information stored therein;

a first configuration path coupled to the link interface and the electrically programmable non-volatile memory, the first configuration path configured to provide the link interface access to the electrically programmable non-volatile memory;

a second configuration path coupled to the electrically programmable non-volatile memory and configured to provide access to the electrically programmable non-volatile memory;

a local serial bus coupled to the electrically programmable non-volatile memory and configured to provide a host system access to the electrically programmable non-volatile memory; and

a memory controller coupled to the link ~~high-speed~~ interface and further coupled to the electrically programmable non-volatile memory through the second configuration path, the memory controller [[and]] having registers into which the memory configuration information is loaded, the memory controller operable to access the electrically programmable non-volatile memory through the second configuration path and further operable to output memory requests in response to receiving memory access requests from the link ~~high-speed~~ interface and in accordance with the memory configuration information loaded in the registers.

36. (Previously presented) The memory hub of claim 35 wherein the electrically programmable non-volatile memory comprises an embedded array of electrically erasable programmable read-only memory.

37. (Cancelled)

38. (Currently amended) A memory sub-system for a host computer system, comprising:

a ~~high-speed~~ bus coupled to the host computer system; and

at least one memory module, each memory module having a plurality of memory devices and further having a memory hub coupled to the bus ~~high-speed link~~ and the plurality of memory devices to control access to the memory devices, the memory hub including a memory controller coupled to the plurality of memory devices of the memory module to output memory access requests to the plurality of memory devices, the memory hub [[and]] further including a configuration memory coupled to a local serial bus operable to provide the host computer system with access to the configuration memory and further coupled to the memory controller through a configuration path to provide the memory controller with memory module configuration information stored in the configuration memory and to store memory module configuration information written to the configuration memory.

39. (Previously presented) The memory sub-system of claim 38 wherein the electrically programmable non-volatile memory comprises an embedded array of electrically erasable programmable read-only memory.

40. (Cancelled)

41. (Currently amended) The memory sub-system of claim 38 wherein the memory hub further comprises a link ~~high-speed~~ interface coupled to the ~~high-speed~~ bus and the memory controller to provide access to the memory module by the host computer system.

42. (Previously presented) The memory sub-system of claim 38 wherein the memory module configuration information comprises at least one of timing information for the plurality of memory devices of the memory module, memory module configuration data, memory device type, and manufacturer data.

43. (Currently amended) A memory module, comprising:

a plurality of memory devices; and

a memory hub coupled to the plurality of memory devices, the memory hub having a link ~~high-speed~~ interface for receiving memory access requests, an electrically erasable programmable non-volatile memory having memory configuration information for the plurality of memory devices stored therein, and a local serial bus coupled to the electrically erasable programmable non-volatile memory and configured to provide a host system access to the electrically erasable programmable non-volatile memory, the memory hub further having a memory controller coupled to the link ~~high-speed~~ interface and further coupled to the electrically erasable programmable non-volatile memory through a configuration path to output memory requests to the plurality of memory devices in response to receiving memory access requests from the link ~~high-speed~~ interface and in accordance with the memory configuration information stored by the electrically erasable programmable non-volatile memory.

44. (Currently amended) The memory module of claim 43 wherein the electrically erasable programmable non-volatile memory comprises an embedded non-volatile memory integrated with the memory controller and the link ~~high-speed~~ interface.

45. (Cancelled)

46. (Previously presented) The memory module of claim 43 wherein the memory configuration information comprises at least one of timing information for the plurality of memory devices of the memory module, memory module configuration data, memory device type, and manufacturer data.

47. (Currently amended) A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a system memory port and a peripheral device port;

an input/output channel coupled to the system controller; and

a memory module coupled to the system memory port of the system controller, the memory module comprising:

a plurality of memory devices; and

a memory hub coupled to the plurality of memory devices, comprising:

a link ~~high-speed~~ interface for receiving memory access requests from the system controller;

an electrically programmable non-volatile memory having memory module configuration information for the plurality of memory devices stored therein;

a first configuration path coupled to the link interface and the electrically programmable non-volatile memory, the first configuration path configured to provide the link interface access to the electrically programmable non-volatile memory;

a second configuration path coupled to the electrically programmable non-volatile memory and configured to provide access to the electrically programmable non-volatile memory;

a local serial bus coupled to the electrically programmable non-volatile memory and configured to provide a host system access to the electrically programmable non-volatile memory; and

a memory controller coupled to the link ~~high-speed~~ interface and further coupled to the electrically programmable non-volatile memory through the second configuration path, the memory controller operable to access the electrically programmable non-volatile memory through the second configuration path and further operable to output memory requests to the plurality of memory devices in response to receiving memory access requests from the link ~~high-speed~~ interface and in accordance with the memory configuration information stored by the electrically programmable non-volatile memory.

48. (Previously presented) The processor-based system of claim 47 wherein the electrically programmable non-volatile memory comprises an embedded array of electrically erasable programmable read-only memory.

49. (Cancelled)

50. (Previously presented) The processor-based system of claim 47 wherein the memory configuration information comprises at least one of timing information for the plurality of memory devices of the memory module, memory module configuration data, memory device type, and manufacturer data.

51. (Currently amended) A method for configuring a memory sub-system having a plurality of memory modules, each ~~at least one~~ memory module having a plurality of memory devices, the method comprising:

accessing a plurality of electrically programmable non-volatile memories storing configuration information for a respective one of the memory modules, the configuration information including at least one of timing information for memory devices of the respective memory module, memory module configuration data, memory device type, and manufacturer data; and

copying the configuration information from each of the plurality of electrically programmable non-volatile memories into configuration registers of a respective memory controller, each memory controller corresponding to one of ~~a corresponding plurality of memory controllers~~ the memory modules.

52. (Previously presented) The method of claim 51, further comprising providing the respective configuration information from the plurality of electrically programmable non-volatile memories to registers of a system memory controller to which each of the plurality of electrically programmable non-volatile memories is coupled.

53. (Previously presented) The method of claim 52 wherein providing the respective configuration information to registers of a system memory controller comprises coupling the respective configuration information to a serial bus to which the system memory controller is coupled.

54. (Previously presented) The method of claim 52 wherein accessing a plurality of electrically programmable non-volatile memory comprises accessing a plurality of electrically erasable programmable read-only memory.

55. (Previously presented) The method of claim 52 wherein accessing a plurality of electrically programmable non-volatile memory comprises accessing a plurality of embedded non-volatile memories.

56. (Previously presented) The method of claim 52 wherein copying the configuration information comprises copying at least one of timing information for a plurality of memory devices of a memory module, memory module configuration data, memory device type, and manufacturer data.

57. (Currently amended) A method for initializing a memory sub-system having a plurality of memory modules, each ~~at least one~~ memory module having a plurality of memory devices, the method comprising:

loading configuration registers of a plurality of memory hubs with the configuration information including at least one of timing information for memory devices of the memory module, memory module configuration data, memory device type, and manufacturer data, each memory hub corresponding to a respective one of the memory modules and the configuration information provided by a respective one of a plurality of embedded electrically programmable non-volatile memories integrated in the respective memory hub.

58. (Previously presented) The method of claim 57, further comprising providing the configuration information from the plurality of embedded electrically programmable non-volatile memories to registers of a system memory controller to which each of the plurality of embedded electrically programmable non-volatile memories are coupled.

59. (Previously presented) The method of claim 57 wherein loading configuration registers of a plurality of memory hubs with the configuration information comprises loading configuration registers of the plurality of memory hubs with at least one of memory module capacity and memory module clock speed.

60. (Previously presented) The method of claim 57 wherein loading configuration registers of a plurality of memory hubs comprises loading configuration registers of a memory controller integrated in a respective one of the plurality of memory hubs.